ABV-Indian Institute of Information Technology & Management, Gwalior

Mid Sem Examination

Sub: CoA(CS-202) **Date:** Sep 25, 2024 **Class:** BCS+BEE Sem III

Time: 2 hours **Max. Marks:** 30

Note: Attempt **all** questions.

1. Design a 3 bit even parity generator circuit by first realizing its truth table and expression, with minimum number of gates. [2+2]

2. Implement the following code, using common bus and tri-state buffers.

   j: M← A

   k: A← Y

   l: R← M

   n: Y←R, M←R

   Assume M, A, R, Y are one but D flip flops. [4]

3. The 8-bit registers A, B, C & D are loaded with the value $(F2)_H$, $(FF)_H$, $(B9)_H$ and $(EA)_H$ respectively. Determine the register content after the execution of the following sequence of micro-operations sequentially.

   a. $A \leftarrow A + B,\ \ C \leftarrow C + Shl(D)$

   b. $C \leftarrow C \wedge D,\ \ B \leftarrow B + 1$

   c. $A \leftarrow Shr(B) \oplus Cir(D)$ [6]

4. Give the hardware realization of 4-bit arithmetic circuit capable of doing addition, subtraction, increment, decrement operations. Give the function table. [3+2]

5. A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

   a. How many bits are there in the operation code, the register code part and the address part?

   b. Draw the instruction word format and indicate the number of bits in each part.

   c. How many bits are there in the data and address inputs of the memory? [3]

6. What is difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? [1+2]

7. What is instruction cycle? Implement the RTLs of fetch phase. [2+3]