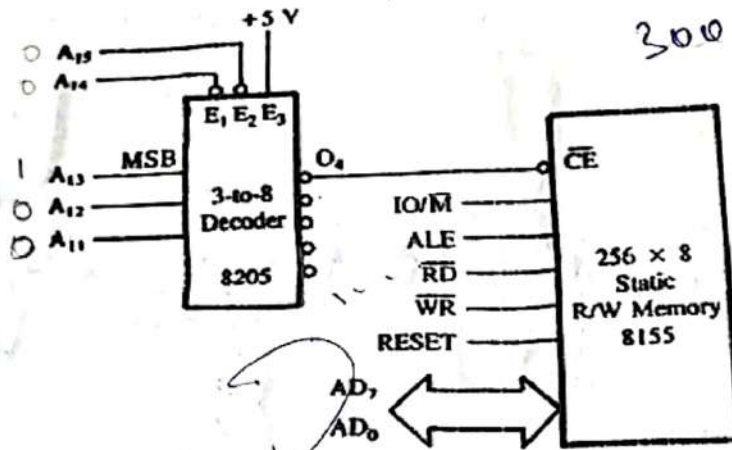**MINOR EXAMINATION-2025**     Marks: 30 (10X2+ 4X1+2+4)

**Course Name**: Microprocessor and Interfacing (EE206)

**Instructions:** (a) Calculators are permitted for use. (c) For any doubts, write them on the answer sheet marked with an asterisk (*) if unresolved during the exam. (d) Attempt all questions (e) Write answer in Hex code.

1. Calculate the number of memory chips needed to design an 8K-byte memory, given that each memory chip is of size 1024 × 1. If a system has a 32-bit address bus, how much memory can the system address?

2. A 2K-byte 8085 memory chip begins at the address location 3000H. Specify the address of the last memory location.



3. Find Memory address range of 8155. (Unconnected pins considered as 0)

4. What are the types of registers in 8085 and which can make pair?
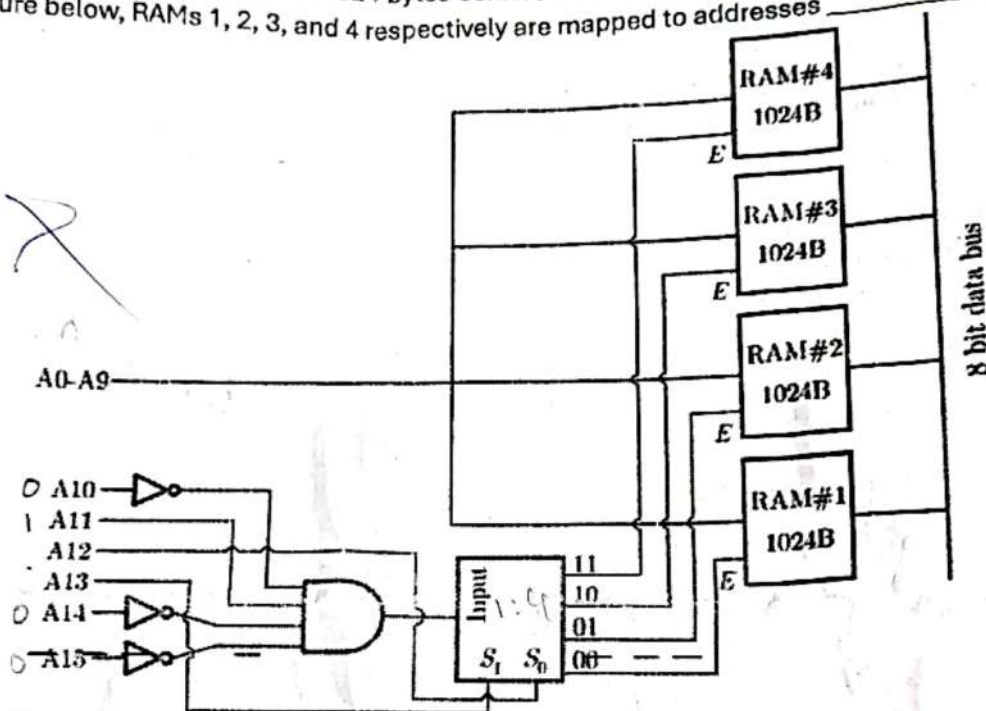
```
MVI B, 91H
MVI C, A8H
MOV A, B
ORA C
OUT PORT1
HLT
```

5. The final content of the accumulator. The status of the Sign (S), Zero (Z), and Carry (CY) Flags after the execution of each instruction (show calculations).

6. Write an assembly language program to interchange (swap) the contents of two memory locations 2000 H and 3101 H. (only correct and complete instructions will be considered).

7. Write an 8085 program to add two 8-bit numbers stored in memory locations 2000H and 2001H. Store the result in 2002H.

8. Assume accumulator contains AAH and CY = 0, Illustrate the contents of the accumulator after execution of the instruction RAL twice.

9. (a) What will be the content of the accumulator after executing the following instructions?

MVI A, 55H

XRI FFH

(b) What happens after executing the following?

LXI H, 2000H

INX H

10. There are four chips each of 1024 bytes connected to a 16-bit address bus as shown in the figure below, RAMs 1, 2, 3, and 4 respectively are mapped to addresses _____ .



11. Which register in the 8085 microprocessor is used to store the result of arithmetic and logic operations? Temporary

12. Why 8085 is called 8-bit processor?

13. Which of the following statements is true?

    a) Harvard architecture is slower than Von Neumann architecture

    b) Von Neumann architecture has separate memory for data and instructions

    c) Harvard architecture allows simultaneous instruction and data access

    d) Von Neumann architecture eliminates memory bottlenecks microprocessor?

14. The first machine cycle of the instruction is .opcode fetch

15. Design a simple embedded system for a digital thermometer. What components will you use and how will they interact?

16. Identify machine cycle machine cycle and T-states for the following instruction

    a) MOV B, C (b) MVI A, 64H (c) LXI 1050H (d) RAL