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CSE207

[ET]

END SEMESTER EXAMINATION : NOV.–DEC., 2019

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION

Time : 3 Hrs. *Maximum Marks : 60*

Note: ***Attempt questions from all sections as directed. Use of Simple Calculator is allowed.***

SECTION – A (24 Marks)

Attempt any **four** *questions out of* **five.**
Each question carries **06** *marks.*

1. (a) Construct a 16 × 1 multiplexer with two 8 × 1 multiplexer and one 2 × 1 multiplexer. Use block diagram for three multiplexers. (3)

   (b) The following memory units are specified, how many address lines and data lines are needed in each case?

   (i) 6G × 34

   (ii) 2K × 16

   (iii) 16M × 32 (3)

P.T.O.

2. Distinguish between memory mapped IO and IO mapped IO, how many devices can be mapped in each case?

3. Explain, how processor executes an instruction with help of flow chart. Also, explain how it handles a situation if it gets disturbed while executing an instruction?

4. How can we use multiplexer to design a full adder? Explain with help of diagram and truth table.

5. (a) Differentiate between direct and indirect addressing, How many references are need to memory for each type of instruction to bring operand to the processor register. (3)

   (b) Write micro-operations for following instruction

   (i) BSA

   (ii) ISZ

   (iii) BUN (3)

SECTION – B (20 Marks)

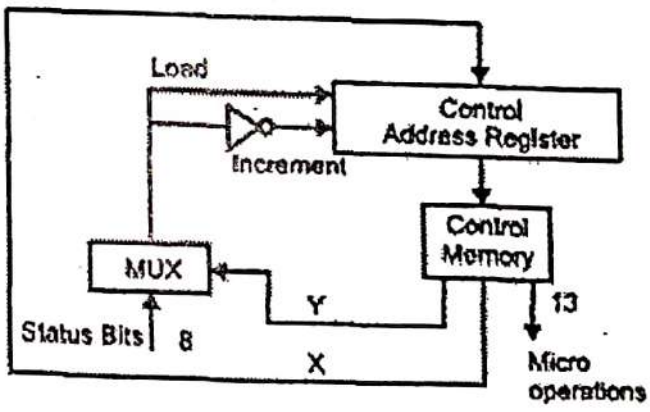
Attempt any **two** *questions out of* **three.**
Each question carries **10** *marks.*

6. Explain Booth's algorithm for multiplying binary integer in signed 2's complement representation.

7. (a) Register A holds the 8 bit binary 11011001. Determine the B operand and logic micro-operation to be performed in order obtain following data in A (5)

(i) 01101101 (ii) 11111101

(b) The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits (refer figure below) in the inputs of the MUX. How many bits are there in the X and Y fields, and what is the size of the control memory in number of words? (5)



8. (a) Differentiate between instruction and arithmetic pipeline. (5)

(b) Explain, how address mapping takes place between physical memory and logical memory with help of an example. (5)

P.T.O.

SECTION – C (16 Marks)

(Compulsory)

9. (a) The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. Find the number of clock cycles required for completion of execution of the sequence of instruction. (6)

(b) A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, how many bits TAG filed will have? (5)

(c) For each of the following 16 bit instructions, give the equivalent four-digit hexadecimal code and explain in your own words, what it is that the instruction is going to perform?

(i) 1011 0001 0101 0100
(ii) 0001 0000 0101 0100
(iii) 0111 0000 0101 0100 (5)