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CSE207 Enrol. No. A2305220433

[ET]

END SEMESTER EXAMINATION : NOV.–DEC., 2021

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION

Time : 3 Hrs. *Maximum Marks : 60*

Note: ***Attempt questions from all sections as directed.***

SECTION – A (24 Marks)

Attempt any **four** *questions out of* **five**.
Each question carries **06** *marks.*

1. The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.

   (a) What is the instruction that will be fetched and executed next?

   (b) Show the binary operation that will be performed in the AC when the instruction is executed.

P.T.O.

(c) Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the values of E, I, and the sequence counter SC in binary at the end of the instruction cycle.

2. A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.

3. Draw a space-time diagram for a six-segment pipeline. A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

4. The transformation of data from main memory to cache memory is mapping. Discuss mapping procedures while considering the organization of a cache memory?

5. Explain the system bus structure and multiport memory organization for multiprocessors.

SECTION – B (20 Marks)

Attempt any **two** *questions out of* **three**. *Each question carries* **10** *marks.*

6. Discuss Booth multiplication algorithm and show the contents of registers E, A, Q, and SC during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). The signs are not included.

7. Design a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

   The 8-bit registers AR, BR, CR, and DR initially have the following values:

   AR 11110010, BR 11111111, CR 101 11001, DR 11101010.

   Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

   (1) AR ← AR + BR Add BR to AR

   (2) CR ← CR AND DR, AND DR to CR

   (3) BR ← BR + 1 increment BR

   (4) AR ← AR – CR, Subtract CR from AR

P.T.O.

8. Discuss associative memory in detail. Obtain the Boolean function for the match logic of one word in an associative memory taking into consideration a tag bit that indicates whether the word is active or inactive.

SECTION – C (16 Marks)

(Compulsory)

9. (a) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages.

S	Cin =0	Cin =1
0	D=A+B	D= A+1
1	D= A-1	D=A+B'+1

(6)

(b) Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input.

$xyT_0 + T_1 + yT_3 : AR \leftarrow AR + 1$ (4)

(c) Design an array multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders.

(6)

(1000)