[No. of Printed Pages – 4]

SSE241

CSE207

[ET]

Enrol. No. .....

SPECIAL SUPPLEMENTARY EXAMINATION :
AUGUST, 2022

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION

Time : 3 Hrs. *Maximum Marks : 60*

Note: ***Attempt questions from all sections as directed.***

SECTION – A (24 Marks)

Attempt any **four** *questions out of* **five.**
Each question carries **06** *marks.*

1. Design a 4-bit combinational circuit Decrementer using four full-adder circuits.

2. Discuss the concept of Instruction Code with proper example.

3. Explain Booths Algorithm? Using Booths algorithm evaluate (+8) X (–)9.

P.T.O.

4. Explain the read and write operations in Associative memory.

5. Construct a diagram for a 4×4 omega switching network. Show the switch setting required to connect input 3 to output 1.

SECTION – B (20 Marks)

Attempt any **two** *questions out of* **three.**
Each question carries **10** *marks.*

6. (a) What is cache coherence, and why is it important in shared-memory multiprocessor systems? How can the problem be resolved with a snoopy cache controller? (7)

   (b) Determine by means of truth table the validity of DeMorgan's Theorem for three variables.

   $(ABC)' = A' + B' + C'$ (3)

7. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for such type oi instruction to bring an operand into a processor register?

8. How interrupts cause a break in the normal execution of a program? Differentiate among external internal and software interrupts.

SECTION – C (16 Marks)

(Compulsory)

9. (a) The 8-bit registers AR, BR, CR, and DR initially have the following values:

AR 11110010

BR 11111111

CR 10111001

DR 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

AR <-- AR + BR	Add BR to AR
CR <-- CR ^ DR, BR <-- BR + 1	AND DR to CR, increment BR
AR <-- AR – CR	Subtract CR from AR

(10)

(b) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes? (3)

(c) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? (3)