[No. of Printed Pages – 8] 1013

CSE207 Enrol. No. .....

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END SEMESTER EXAMINATION : NOVEMBER-DECEMBER, 2023

DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION

Time : 3 Hrs. *Maximum Marks : 60*

Note: ***Attempt questions from all sections as directed.***

SECTION – A (24 Marks)

Attempt any **four** *questions out of* **five**.
Each question carries **06** *marks.*

1. What is associative memory, what additional logic is required to give a no-match result for a word in an associative memory when all key bits are zeros?

2. What is the need of processor registers whem primary and secondary memory is there in computer? The 8-

bit registers AR, BR, CR, and DR initially have the following values:

AR 11110010
BR 11111111
CR 10111001
DR 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations(registers take updated value in each step)

AR <- AR + BR
CR <- CR ^ DR, BR <- BR + 1
AR <-AR - CR

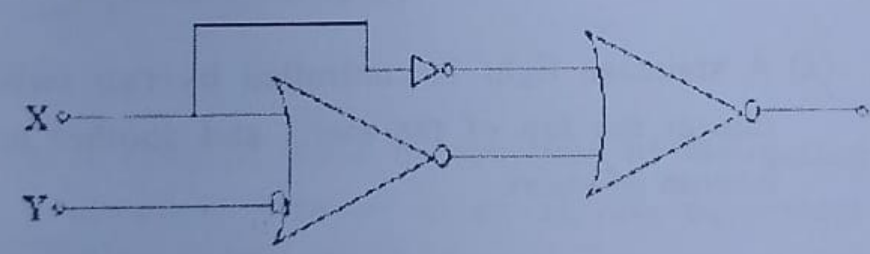
3. (a) Starting from an initial value of R =11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. (2)

(b) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages.

S	$C_{in} = 0$	$C_{in} = 1$
0	$D = A + B$ (add)	$D = A + 1$ (increment)
1	$D = A - 1$ (decrement)	$D = A + \overline{B} + 1$ (subtract)

(4)

4. Draw the minimized ~~circuit~~ boolean expression for Figure given below



5. (a) For the given16-bit iitstructions, give the equivalent four-digit hexadecimal code and explain in your own words what it is that the instruction is going to perform. (3)

1011_3

(a) 0001 0000 0010 0100

(b) 1011 0001 0010 0100

(c) 0111 0000 0010 0

(b) Draw a timing diagram for that SC is cleared to 0 at time T3 if control signal C7 is active.

C7T3: SC<-0 (3)

SECTION – B (20 Marks)

Attempt any **two** *questions out of* **three**.

Each question carries **10** *marks*.

6. (a) A staircase light is controlled by two switches one at the top of the stairs and another at the bottom of stairs

(i) Make a truth table for this system.

(ii) Write the logic equation .

(iii) Realize the circuit using AND-OR gates (3)

XOR

(b) An instruction goes through different phases, write names of those phases and explain each phase in detail with help of flow chart. Also explain how instruction cycle is different from interrupt cycle. (7)

7. (a) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated? (3)

(b) How pipelining can be used in achieving parallel processing? Draw a space-time Dignam for a six-segment pipeline showing the time it takes to process eight tasks. (7)

8. (a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

(i) What should be the value of the relative address field of the instruction (in decimal)?

(ii) Determine the relative address value in binary using 12 bits. (Why must the number be in 2's complement?)

(iii) Determine the binary value in PC after the fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address calculated in part (b) is equal to the binary value of 500. (6)

(b) Differentiate between following

(i) hardwired control and micropraogrammed control

(ii) instruction and arithmetic pipeline (4)

SECTION – C (16 Marks)

(Compulsory)

9. (a) Consider a 3-stage pipelined processor having a delay of 10 ns (nanoseconds), 20 ns, and 14 ns, for the first, second, and the third stages, respectively. Assume that there is no other delay and the processor does not suffer from any pipeline

$\frac{10+20+14}{100} = \frac{44}{100} = 0.44$

$0.44 + 44 = 44.44$

hazards. Also assume that one instruction is fetched every cycle.find the total execution time for executing 100 instructions on this processor. (6)

(b) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is (a) a computational type requiring an operand from memory; (b) a branch type (4)

(c) A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped 1/0 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

(i) How many RAM and ROM chips axe needed?

(ii) Draw a memory-address map for the system.

(iii) Give the address range in hexadecimal for RAM, ROM, and interface (6)