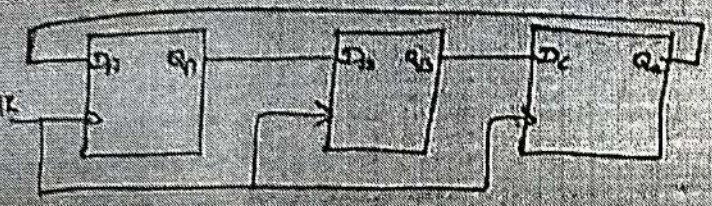
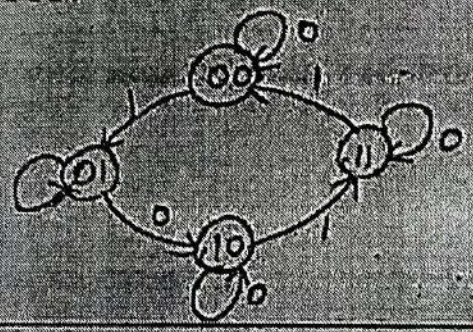
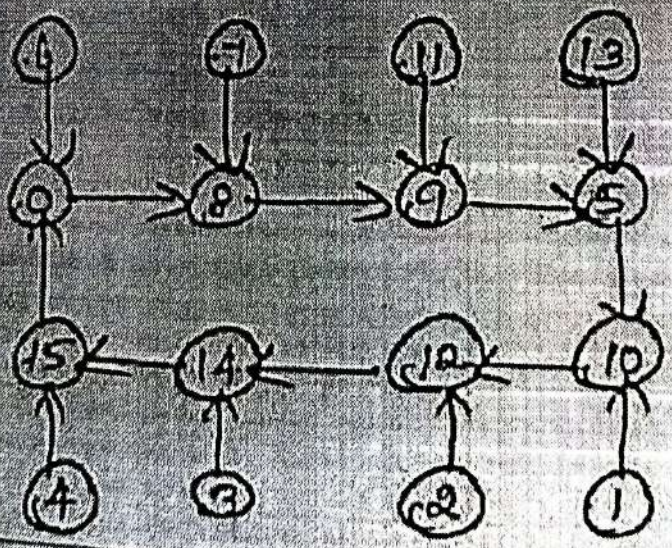
Title		Questions	Marks	L
I & Basic Concepts	1	Simplify the following Boolean function $f(W,X,Y,Z)=\sum m(0,1,2,5,6,7,8,9,10,14)$ using Quine-McCluskey tabular method.	16	
	2	Simplify the Boolean expression using K-Map and realize the expression using gates. i. $(w,x,y,z)=\sum(1,2,3,5,9,12,13,14,15)$. ii. $F(A,B,C,D)=\sum m(0,1,2,3,4,5,8,10,12)$	16	
	3	Convert the followings: i.$(1234)_{10}=(\ )_2$ ii.$(675)8=(\ )_2$ iii.$(A5B6)_{16}=(\ )_2$ iv.$(1010110001000101)_2=(\ )_{16}$	16	
	4	Convert the followings: i $(1234)_{10}=(\ )_2$ ii. $(675)8=(\ )_2$ iii. $(A5B6)_{16}=(\ )_2$ iv. $(1010110001000101)_2=(\ )_{16}$	16	
	5	Find the minimal expression of the following function using K-map method $(A,B,C,D)=\sum m(0,1,2,4,5,8,9,13,14)$.	16	
	6	Convert the following SOP to Sum of minterms. (i)F=AC+BC+AB (ii)F=A+B'C	16	
	7	Reduce the following Boolean expression (i)y=ΠM(0,1,4,5,6,8,9,13,14) (ii)y=∑(1,2,5,6,8,9) using K-Map	16	
Combinational Logic Circuits	1	Design and implement the Half adder and Full adder.	16	
	2	A Majority gate is a digital circuit whose output is equal to 1 if the majority of inputs are 1's. The output is 0 otherwise. Using a truth table, find the Boolean function implemented by a 3-input majority gate. Simplify the function and implement with gates.	16	
	3	Explain in detail about 2-bit Magnitude Comparator	16	
	4	Define Decoder. Design and implement a 3 to 8-line Decoder.	16	
	5	Design and implement an 8:1 and 4:1 Multiplexer.	16	
	6	Implement the following Boolean expression using suitable multiplexer, F (A, B, C, D) =∑ (0,1,3,4,8,9,15).	16	

7	Design an Binary to Gray code converter.	16	L3	
1	Draw the logic diagram of a JK – flip flop and explain its operation.	16	L2	B
2	Design and implement Mod-10 Synchronous counter using JK-FFs.	16	L4	A
3	Design a synchronous counter that counts the sequence 0-7-5-6-1-2-0 using JK flip flop	16	L2	A
4	A sequential circuit with delay flip flop A and B has two inputs x & y and output z is specified by the following next state equation and output equation. Draw the state diagram and logic diagram $A(t+1) = x'y+xa$ $B(t+1) = x'b+xa$ $Z = b$	16	L2	
5	Draw the state table, state diagram for the sequential circuit shown below 	16	L4	
6	Design a synchronous sequential circuit for the below state diagram using JK-FF. 	16	L4	
7	Design a counter that counts the following sequence. 	16	L4	
8	Design a mod-6 or divide by 6 Down counter using and JK flip-flops.	16	L4	
9	Design a mod-5 down counter or divide by 5 counter using and T-flip flop.	16	L4	
	Design an asynchronous			