End-Term Examination
(CBCS)(SUBJECTIVE TYPE)(OffLine)
Course Name: B. Tech AI&ML and CSE-AI, Semester: 1
(December, 2023)

Subject Code: BAI – 103	Subject: Computer organization & Architecture
Time :3 Hours	Maximum Marks :60

Note:Q. 1 is compulsory. Attempt one question each from the Units I, II, III & IV.

Q1		(2.5*8=20)	
	(a) Explain the working of SR flip flop with its disadvantages. Give one example of the use of S-R flip flop.		
	(b) Explain any five laws of Boolean Algebra.		
	(c) Write the format of Memory Reference, I/O Reference and Register Reference Instruction.		
	(d) What do you mean by the following terms? (i) AR ← m[AR] (ii) Micro-Operation		
	(e) Explain Parallel processing.		
	(f) Define floating point representation with an example.		
	(g) What is the basic Characteristic of Cache Memory ?		
	(h) What is meant by Mapping ? Name three types of Mapping procedures.		
	UNIT-I (10 Marks)		
Q2	a)Simplify using De Morgan's Law: i) ((A'+C)(AB)')' ii) (AB')' (B'+C) b) Explain the working of a 4-bit asynchronous binary counter with logic diagram, timing diagram and truth table.	(5,5)	
Q3		(5,5)	
	(i) Implement the following multiplexer : $f(A,B,C) = \bar{A}B+BC+\bar{A}C$ Draw the block diagram also. (ii) What is a Counter ? State the two different types of Counters. Explain the working of any one type of a counter		
	UNIT-II (10 Marks)		
Q4	a)A computer uses a memory unit with 256K words of 32-bits each. A binary instruction code is stored in one word of memory. The instruction has 4 parts: an indirect bit, opcode, a register code to specify one of the 64 registers and an address part. (i) How many bits are there in the opcode, register code part and address part. Justify your answer. (ii) Draw the instruction word format and indicate the number of bits in each part. (iii) How many bits are there in the data & address inputs of the memory?Why? b) What are the 2 types of control unit? Explain any 1 of them in detail with suitable diagram.	(5,5)	
Q5	(i) Evaluate $x = (A+B) \times (C+D)$ with the help of ONE-ADDRESS instruction and ZERO—ADDRESS instruction.	(5,2.5,2.5)	

	(ii) For a memory unit with size 4096×16, how many bits are used to specify an address? How many bits are available for the operation code and specify how many operations are possible. (iii) Explain different phases of an Instruction cycle.	
	UNIT-III (10 Marks)	
Q6	a) A no pipeline system takes 50 ns to process a task. The same task can be processed in 6 segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of pipeline for 100 tasks. b) Explain branch instruction hazard in detail with suitable diagram. c) Show the step by step multiplication process using BOOTH algorithm for: (+15) x (+13). Assume 5-bit registers that hold the numbers and the multiplicand as (+15).	(2,3,5)
Q7		
	(i) Explain the term pipelining and draw the pipeline structure for : Ai+Bi × Di for i=1,2.....6. (ii) Draw the hardware Algorithm for "multiplication of signed magnitude data". Multiply 10011 multiplicand with 10001 multiplier with successive multiplication as well as hardware algorithm process.	(5,5)
	UNIT-IV (10 Marks)	
Q8	Write short notes on: a) Memory hierarchy in a computer system b) Content Addressable Memory or Associative Memory	(5,5)
Q9		
	(i) Explain Virtual Memory Organization and Associative Memory. (ii) What is meant by the terms. • Handshaking • Destination—Initiated Transfer.	(5,5)