NATIONAL INSTITUTE OF TECHNOLOGY KURUKSHETRA

THEORY EXAMINATION

Question paper

08 DEC 2018

**onth and Year of the Examination:** Dec. 2018 **Roll No:** _____

**Subject:** Computer Organization and Architecture **Branch:** INFORMATION TECHNOLOGY

**Course:** B.Tech **Subject Code:** ITPC-29

**Time Duration:** Three (3) Hours **Semester:** III

**Total No. of Questions:** Six (6) **Maximum Marks:** 50

**Number of Questions to be Attempted:** Five (5)

*Note:*

*Attempt all parts of question together at one place. Marks allotted for each question are shown on the right hand margin. Write your answer with question no.*

*. The Candidates, before starting to write the solutions, should please check the question paper for any discrepancy, and also sure that they have been delivered the question paper of right course no. and right subject title.*

*. Unless stated otherwise, the symbols have their usual meanings in context with the subject. **Assume suitably and state, ditional data required, if any.***

| o. | QUESTIONS | Marks |
|---|---|---|
| - | (a) What are typical characteristics of a RISC instruction set architecture?<br>(b) Show how the MRI and non-MRI tables can store in memory.<br>(c) Distinguish between loosely coupled and tightly coupled MIMD computer. | 2+4+4 = 10 |
| | (a) What are the basic differences between branch instruction and a call subroutine instruction? Give the suitable example.<br>(b) What are the addressing modes and why are there so many different modes? Explain with suitable examples. | 4+6 = 10 |
| | (a) How do you improve the cache performance?<br>(b) Define the following terms: microinstruction, microoperation, microroutine, control word and control store.<br>(c) What are the differences between isolated I/O and memory mapped I/O? Give the suitable example. | 2+4+4 = 10 |
| | a) Differentiate between instruction cycle and interrupt cycle. Give the suitable xample.<br>) Explain the methods of Asynchronous data transfer with suitable diagram. | 4+6 = 10 |
| | escribe in details for organization in CPU with necessary diagrams and examples. | 10 |
| | raw the block diagram with explanation for connection of the registers and memory the basic computer to a common bus system. | 10 |