THEORY EXAMINATION

Question Paper

0 8 DEC 2018

Month and Year of the Examination: **Nov/Dec-2018**

Programme....**B.Tech**

Semester.....**3rd** .....

Subject...**Computer Organization& Architecture**

Course No..... **CSPC-29** ...

Total number of questions given.....**8**.....

Maximum Marks...**50**.....

Number of Questions to be attempted...**5**...

Time allowed...**3 hrs**.....

Q1. (a)	Explain about the memory hierarchy in a computer system with block diagram. Which of the fundamental RAM technologies has a faster read access time and a faster write time?	**05 Marks**
(b)	What is the transfer rate of an eight-track magnetic tape whose speed is 120 inches per second and whose density is 1600 bits per inch? The number of characters/second that can be transmitted to the memory from the tape is denoted by which term? Tape drive is connected to and controlled by which system? Magnetic tape which type of access device?	**05 Marks**
Q2. (a)	Explain the different types of mapping procedures in the organization of cache memory with block diagram.	**04 Marks**
(b)	A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. (a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address. (b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176 All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.	**06 Marks**
Q3. (a)	Explain in detail about the working of Flash Memory? What are Removable Flash Memory Cards and their Applications (at least 3)? What are the Flash Memory Standards?	**06 Marks**
(b)	Assume we have the following values stored in memory and R1 storing 200. Location Value 1000 1300 1100 1200 1200 800 1300 1200 What is loaded into the AC using the MARIE instruction Load 1000 when using each of the following addressing modes? a. Immediate b. Direct c. Indirect d. Indexed	**04 Marks**
Q4. (a)	Describe about Instruction Cycle state diagram? If memory address register (MAR) is k bits long, then what should be its processor address? Define three instructions of register-reference and Memory-reference? What is the major difference between the EPROM and ROM circuitry?	**06 Marks**

(b)	Write a program to evaluate the arithmetic statement: $X = (A - B + C * (D * E - f)) / (G + H * K)$ a. Using a general register computer with RISC instructions. b. Using a general register computer with two instructions. c. Using an accumulator type computer with one address instructions. d. Using a stack organized computer with zero-address operation instructions.	04Ma
Q5. (a)	Explain the interrupt cycle with the help of flow chart? When a device interrupt occurs, how does the processor determines which device issued the interrupt?	04Marks
(b)	A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. a) How many bits are there in the operation code, the register code part, and the address part? b) Draw the instruction word format and indicate the number of bits in each part. c) How many bits are there in the data and address inputs of the memory.	06 Marks
Q6. (a)	Explain in detail the term "Pipelining" also draw the block diagram of Arithmetic Pipeline and Instruction Pipeline?	06 Marks
(b)	A computer has 32-bit instructions and 12-bit addresses. There are 250 two address instructions. How many one address instructions can be formulated? Give five examples of external interrupts and five examples of internal interrupts. What is the difference between a software interrupt and a subroutine call?	04Marks
Q7. (a)	What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processsor register? How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is (a) a computational type requiring an operand from memory; (b) a branch type.	06 Marks
(b)	A virtual memory system has an address space of 8k words, memory space of 4k words and Page & Block size of 1k words. The following page reference changes occur during a given time interval. 4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7 Determine the four pages that are resident in main memory after each Page reference change if the replacement algorithm used is (i)FIFO (ii) LRU.	04Marks
Q8.	Why does DMA have priority over the CPU when both request a memory transfer? What is the function of DMA? What is the advantage with DMA? Are there any alternatives to DMA? How does it work in practice? Why are the read and write control lines in a DMA controller bi directional?	10Marks