NATIONAL INSTITUTE OF TECHNOLOGY, KURUKSHAETRA
THEORY EXAMINATION
Question Paper

Month and Year of Examination: Nov.-Dec. 2020
Programme: B. Tech Semester: III[rd]
Subject: Computer Organization and Architecture
Course No: ITPC 29 Maximum Marks:50
Number of Questions to be attempted: 05 Time Allowed: 2 hrs
Total no. of Questions: 07 Total No of Pages Used: 03

Q1	(i) F(a,b,c,d,e) = Min terms are (0,4,6,8,12,13,14,15,16,17,18,21,24,25,26,28,29,31} obtain the minimal in SOP form (5 marks) (ii) Explain the process of subroutine nesting? (2.5 marks) (iii) Differentiate between combinational and sequential circuits. (2.5 marks)
Q2	(i) The two numbers given below are multiplied using the Booth's algorithm. Multiplicand : 0101 1010 1110 1110 Multiplier: 0111 0111 1011 1101 How many additions/Subtractions are required for the multiplication of the above two numbers? Explain your answer (5 marks) (ii) The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. What is the throughput increase of the pipeline in percent and Why? (5 marks)
Q3	(i) Explain the difference between hardwired and micro programmed control. Is it possible to have a hardwired control associated with control memory? (5 marks) (ii) The instruction pipeline of a RISC processor has the following stages:

	Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write back (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. What is the number of clock cycles required for completion of execution of the sequence of Instructions and why? (5 marks)
Q4	(i) What is address sequencing? Explain the conditional branching and mapping of instruction in it. (5 marks) (ii) Consider a two-level cache hierarchy with L1 and L2 caches. An application incurs 1.4 memory accesses per instruction on average. For this application, the miss rate of L1 cache is 0.1; the L2 cache experiences, on average, 7 misses per 1000 instructions. The miss rate of L2 expressed correct to two decimal places is _____. (5 marks)
Q5	(i)A digital computer has a memory unit of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. (i) How many bits are there in the tag, index, block and words fields of the address format? (ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit. (iii) How many blocks can the cache accommodate? (5 marks) (ii) What is Von Neumann architecture? (5 marks)
Q6	(i) What is difference between isolated and memory mapped I/O? What are advantages and disadvantages of each? (5 marks) (ii) An instruction ADD R1, A is stored at memory location 4004H. R1 is a processor register and A is a memory location with address 400CH. Each

	instruction is 32-bit long. What will be the values of PC, IR and MAR during execution of the instruction? (5 marks)
Q7	(i) A two word instruction is stored in memory at an address designated by symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is (i) Direct (ii)Indirect (iii) Relative (iv) Indexed (5 marks) (ii) Explain how to resolve branch conflicts in Instruction pipeline. (5 marks)