NATIONAL INSTITUTE OF TECHNOLOGY, KURUKSHETRA

THEORY EXAMINATION

Question Paper

Month and Year of the Examination: **NOV/DEC 2020**

Programme: **B.Tech**/M.Tech/MBA/MCA Semester: - **3rd Semester (CO)**

Subject: - **Computer Organization and Architecture**

Course No: - **CSPC-29** Maximum Marks: - **50**

Number of Questions to be attempted: - **5** Time allowed: - **2 Hours**

Total No. of Questions: - **6** Total No. of Pages used: - **3**

Unless stated otherwise, the Symbols have their usual meanings in context with subject. Assume suitably and state, additional data required, if any. The Candidates, before starting to write the solutions, should please check the question Paper for any discrepancy, and also ensure that have been delivered the question paper of right **course no**. and right **subject title**.

1(a) Q — Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz. Assuming the execution of 100 instructions, Calculate the overall CPI. — 5

Instruction Category	Percentage of occurrence	No. of cycles per instruction
ALU	38	1
Load & store	15	3
Branch	42	4
Others	5	5

1(b) Q — Suppose that the same set of benchmark programs considered above were executed on another machine, call it machine B, for which the following measures were recorded. — 5

Instruction Category	Percentage of occurrence	No. of cycles per instruction
ALU	35	1
Load & store	30	2
Branch	15	3
Others	20	5

What is the MIPS rating for the machine considered in the

	previous example (machine A) and machine B assuming a clock rate of 200 MHz?	
2(a) Q	Three enhancements with the following speedups are proposed for a new machine: Speedup(a) = 30, Speedup(b) = 20, and Speedup(c) ¼ 15.Assume that for some set of programs, the fraction of use is 25% for enhancement (a), 30% for enhancement (b), and 45% for enhancement (c). If only one enhancement can be implemented, which should be chosen to maximize the speedup? If two enhancements can be implemented, which should be chosen, to maximize the speedup?	5
2(b) Q	Consider a computer that has a number of registers such that the three registers R0 = 1500, R1 = 4500, and R2 = 1000. Show the effective address of memory and the registers' contents in each of the following instructions (assume that all numbers are decimal). (a) ADD (R0)+, R2 (b) SUBTRACT - (R1), R2 (c) MOV 500 (R0), R2 (d) LOAD #5000, R2 (e) STORE R0, 100(R2)	5
3(a) Q	Discuss the differences between Horizontal Versus Vertical Microinstructions.	4
3(b) Q	Discuss the Internal data movement among registers and between the ALU and registers by using different organizations including one-bus, two-bus, or three-bus organizations.	6
4(a) Q	What is the average access time of a system having three levels of memory, a cache memory, a semiconductor main memory, and a magnetic disk secondary memory, if the access times of the memories are 20 ns, 100 ns, and 1 ms, respectively? The cache hit ratio is 90% and the main memory hit ratio is 95%.	5
4(a) Q	A computer system has an MM consisting of 16 MB 32-bit words. It also has an 8 KB cache. Assume that the computer uses a byte-addressable mechanism. Determine the number of bits in each field of the address in each of the following organizations: a) Direct mapping with block size of one word	5

	b) Direct mapping with a block size of eight words c) Associative mapping with a block size of eight words d) Set-associative mapping with a set size of four block and a block size of one word.	
5(a) Q	Consider the following stream of page requests: 1,2,3,4,5,1,2,3,4,5,1,2,3,4,5. Assume that the main memory consists of FOUR page frames. Show a trace of the status of the page frames in the MM and estimate the hit ratio assuming each of the following page replacement algorithms. (a) FIFO (b) LRU	4
5(b) Q	Discuss the following terms: a) Segmentation b) Segment Address Translation c) Paged Segmentation	6
6(a) Q	What are the advantages and disadvantages of isolated versus memory mapped I/O.	3
6(b) Q	What types of operations is DMA used to accelerate?	2
6(c) Q	Discuss the advantages and disadvantages of the different bus arbitration policies. Prepare a contract table that compares the arbitration techniques from both the implementation and operational aspects.	5

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