NATIONAL INSTITUTE OF TECHNOLOGY, KURUKSHETRA
THEORY EXAMINATION

B. Tech (Information Technology)

III Semester

Computer Organization and Architecture (ITPC-29)

Time Duration :- 50 Minutes **Max. Marks- 15**

Attempt any five questions.

Question No.	Question	Marks
Q1	**Simplify the Boolean expression in SOP form** $f(A,B,C,D,E) = \sum m(0,1,6,7,8,9,21,22,23,29,31)$	**3**
Q2 (a)	**A processor has 64 floating point registers (F0,F1,...,F63) and 16 integer registers(R0,R1,...,R15). It uses 2 byte instruction format. There are four categories of instructions: Type1, type 2, Type 3 and Type 4. Type 1 category consists of four instructions each with three integer operands (3Rs). Type 2 category consists of eight instructions each with 2 floating point register operands (2Fs). Type 3 category consists of fourteen instruction each with one integer register operand and one floating point register operand (1R+1F). Type 4 category consists of N instruction each with floating point register operand (1F). What is the maximum value of N and why?**	**2**
(b)	**In 2's complement, what do all the positive numbers have in common?**	**1**
Q3 (a)	**An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right? Starting from the initial number 10011 100, determine the register value after an arithmetic shift left, and state whether there is an overflow.**	**2**
(b)	**Write the 2's complement for each of the following 5-bit binary numbers.**	**1**

a. 01001_2
b. 01011_2
c. 00111_2

d. 00001_2

Q4 (a) **Represent the following conditional control statement by two register transfer statements with control functions.** **1**

If (P =1) then (RI <-R2) else If (Q =1) then (RI<-R3)

(b) **A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.** **1**

a. How many selection inputs are there in each multiplexer and size of multiplexers are needed?
c. How many multiplexers are there in the bus?

(c) $(F3A7C2)_{16}$ = ($)_8$ **1**

Q5 (a) **Draw the block diagram for the hardware that implements the following statements:** **2**

x + yz: AR <- AR + BR
where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function. (Remember that the symbol + designates an OR operation in a control or Boolean function but that it represents an arithmetic plus in a micro-operation.)

(b) $(F3)_{16}$ = ($)_{10}$ **1**

Q6 The content of *AC* in the basic computer is hexadecimal A937 and the initial value of *E* is 1. Determine the contents of *AC*, *E*, *PC*, *AR*, and *IR* in hexadecimal after the execution of the CLA instruction. Repeat 11 more times, starting from each one of the register-reference instructions. The initial value of *PC* is hexadecimal 021. **3**

CLA	7800	Clear *AC*
CLE	7400	Clear *E*
CMA	7200	Complement *AC*
CME	7100	Complement *E*
CIR	7080	Circulate right *AC* and *E*
CIL	7040	Circulate left *AC* and *E*
INC	7020	Increment *AC*
SPA	7010	Skip next instruction if *AC* positive
SNA	7008	Skip next instruction if *AC* negative
SZA	7004	Skip next instruction if *AC* zero
SZE	7002	Skip next instruction if *E* is 0
HLT	7001	Halt computer