NATIONAL INSTITUTE OF TECHNOLOGY, KURUKSHETRA
THEORY EXAMINATION

B. Tech (Information Technology)

III Semester

Computer Organization and Architecture (ITPC-29)

Time Duration :- 50 Minutes **Max. Marks- 15**

Attempt any five questions.

Question No.	Question	Marks
Q1	(i) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight-bit words. A)How many bits are required for addressing the main memory? B)How many bits are needed to represent the TAG, SET and WORD fields? (ii) A computer has a 256 KB, 4-way set associative, write back data cache with a block size of 32 bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. A)The number of bits in the tag field of an address is _____. B) The size of the cache tag directory is _____ (iii) A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____.	**5**
Q2	Consider an instruction pipeline with five stages without any branch prediction: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Operand Write (OW). The stage delays for IF, ID, OF, EX and OW are 5 nsec, 7 nsec, 10 nsec, 8 nsec and 6 nsec, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 nsec. A program consisting of 12 instructions I1, I2, …, I12 is executed in the pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, what is the time needed to complete the program? Explain	**5**
Q3	(i) Consider a direct-mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order-3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24. Which of the following memory blocks will not be in the cache at the end of the sequence? a)3 b)18 c)20 d)30. Also, calculate the hit ratio and miss ratio. (ii) Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order-4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7.If LRU replacement policy is used, which cache block will have memory block 7?Also,	**5**

calculate the hit ratio and miss ratio.

Q 4 Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate- **5**

1. Pipeline cycle time
2. Non-pipeline execution time
3. Speed up ratio
4. Pipeline time for 1000 tasks
5. Sequential time for 1000 tasks
6. Throughput

Q 5 **A virtual memory has a page size of 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries:** **5**

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses (in decimal) that will cause a page fault if used by the CPU.

Q 6 A hierarchical memory system has the following specification, 20 MB main storage with an access time of 300 ns, 256 bytes cache with access time of 50 ns, word size 4 bytes, page size 8 words. What will be the hit ratio if the page address trace of a program has the pattern 0, 1, 2, 3, 0, 1, 2, 4 following LRU page replacement technique? **5**