Computer Organization and Architecture (CSPC-29) Batch (20-23)

Mid Term (Sessional-3) Max Marks: 20 Time Limit: 40 mins (Upload your hand written solutions in PDF format through Google Classroom only). Those questions, which are not numerical in the question paper, these can be written directly on note book with proper justification. Kindly observe the timing of submission of paper, i.e. 3:40 PM SHARP. The scanned Answer Sheet must be mail to: virender.ranga@ieee.org till 4:00 P.M., if you are not able to upload it on google class room link of your class section. No PDF will be accepted after that in any case.

* Required

Email *

Your email

Name of Student

Your answer

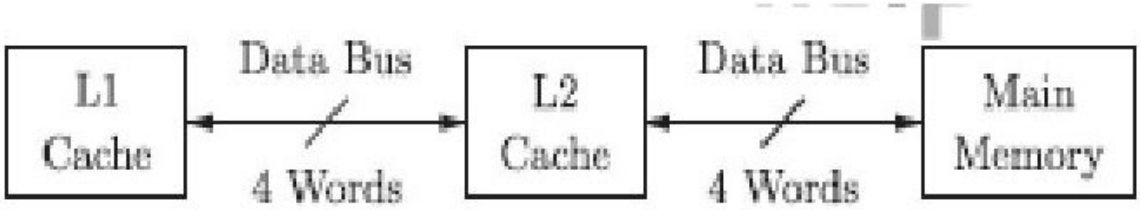
Roll No.

Your answer

Section (1, 2, 3, 4, 5 or 6)

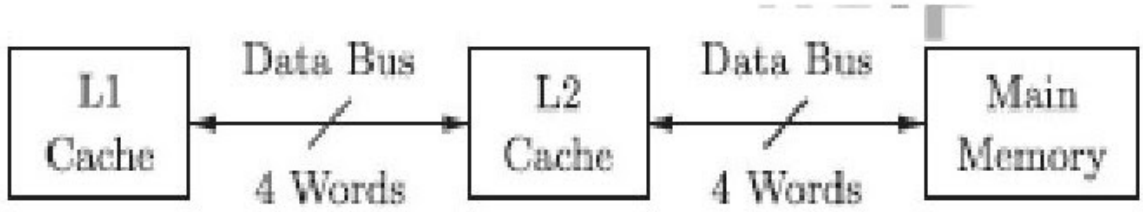
Choose

1 Q: A computer system has an L1 and L2 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size is L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1cache, L2 cache and main memory unity respectively. When there is a miss in L1 cache and a hit in L2 cache, a block is transferred form L2 cache to L1 cache. What is the time taken for this transfer?



- 2 nanoseconds
- 20 nanoseconds
- 88 nanoseconds
- 22 nanoseconds

2 Q: A computer system has an L1 and L2 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size is L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unity respectively. When there is a miss in both L1 cache and L2 cache, first a block is transferred from memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?



- 968 nanoseconds
- 902 nanoseconds
- 888 nanoseconds
- 222 nanoseconds

3. Q: A main memory unit with a capacity of 4 MB is build using 1 M x 1 bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds (ns). The time required to perform one refresh operation on all the cells in the memory unit is

- 100 nanoseconds
- 100 * pow (2,10) nanoseconds
- 100 * pow (2,20) nanoseconds
- 3200 * pow (2,10) nanoseconds

4. Q: Consider a 4 way set associative cache (initially empty) with total16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order: 0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155Which one of the following memory block will NOT be in the cache, if LRU replacement policy is used?

- ○ 216
- ○ 129
- ○ 3
- ○ 8

5. Q: A CPU generally handles the interrupt by executing an interrupt service routine

- ○ As soon as an interrupt is raised
- ○ By checking the interrupt register at the end of fetch cycle
- ○ By checking the interrupt register after finishing the execution of the current instruction
- ○ By checking the interrupt register at fixed time intervals

6. Q: How many 32K X 1 RAM chips are needed to provide a memory capacity of 256K bytes?

- ○ 8
- ○ 32
- ○ 64
- ○ 128

7. Q: Consider a machine with a byte addressable main memory of pow (2, 16) bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 x 50 two-dimensional array of bytes is stored in the main memory stating from memory location 1100h. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses. How many data cache misses will occur in total?

- ◯ 59
- ◯ 48
- ◯ 50
- ◯ 56

8. Q: Consider a 4-way set associative cache consisting of 120 lines with aline size of 64 words. The CPU generates a 20-bit address of a wordin main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

- ◯ 9,6,5
- ◯ 7,7,6
- ◯ 7,5,8
- ◯ 9,5,6

9. Q: Consider a direct mapped cache of size 32 KB with block size 32 bytes.The CPU generates 32- bit addresses. The number of bits needed forcache indexing and the number of tag bits are respectively:

- ◯ 10,17
- ◯ 10,22
- ◯ 5,17
- ◯ 15,17

10. Q: Increasing the RAM of a computer system typically improves performance, because

- ◯ Virtual memory increases
- ◯ Larger RAMs are faster
- ◯ Fewer page faults occur
- ◯ Fewer segmentation faults occur

11. Q: Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for thefollowing sequence of block addresses is 8, 12,0, 12,8

- ◯ 5
- ◯ 4
- ◯ 3
- ◯ 2

12. Q: Which of the following requires a device driver?

- ◯ Disk
- ◯ Cache
- ◯ Register
- ◯ Main memory

Thank you for attending your sessional. All the Best for your result. Marks will be sent to you after verification of your marks based on answers written in PDF solutions file submitted by you through Google Classroom.

Submit Clear form

Never submit passwords through Google Forms.