Computer Organization and Architecture (CSPC-29)

Mid Term (Sessional-1) Max Marks: 20 Time Limit: 40 mins (Submit your hand written solutions in PDF format through Google Classroom, Otherwise marks will not be considered). Start Time: 3 :00 PM, End Time: 3:40 PM (sharp). Total Questions:14

* Required

Email *

Your email

Student' Name

Your answer

Roll No.

Your answer

Section (1, 2, 3, 4, 5 or 6)

Choose

1. A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions? I0 :MUL R2 ,R0 ,R1 R2 ← R0 *R1 I1 :DIV R5 ,R3 ,R4 R5 ← R3 /R4 I2 : ADD R2 ,R5 ,R2 R2 ← R5 + R2 I3 :SUB R5 ,R2 ,R6 R5 ← R2 - R6

- 19
- 15
- 13
- 17

2. Q: Which is the most appropriate match for the items in the first column with the items in the second column (X.) Indirect Addressing (I.) Array implementation (Y.) Indexed Addressing (II.) Writing re-locatable code (Z.) Base Register Addressing (III.) Passing array as parameter

- (A) (X, III) (Y, I) (Z, II)
- (X, II) (Y, III) (Z, I)
- (X, III) (Y, II) (Z, I)
- (X, I) (Y, III) (Z, II)

3. Q: Suppose a processor does not have any stack pointer register. Which of the following statements is true?

- Nested subroutine calls are possible, but interrupts are not
- It can have subroutine call instruction, but no nested subroutine calls
- It cannot have subroutine call instruction
- All sequences of subroutine calls and also interrupts are possible

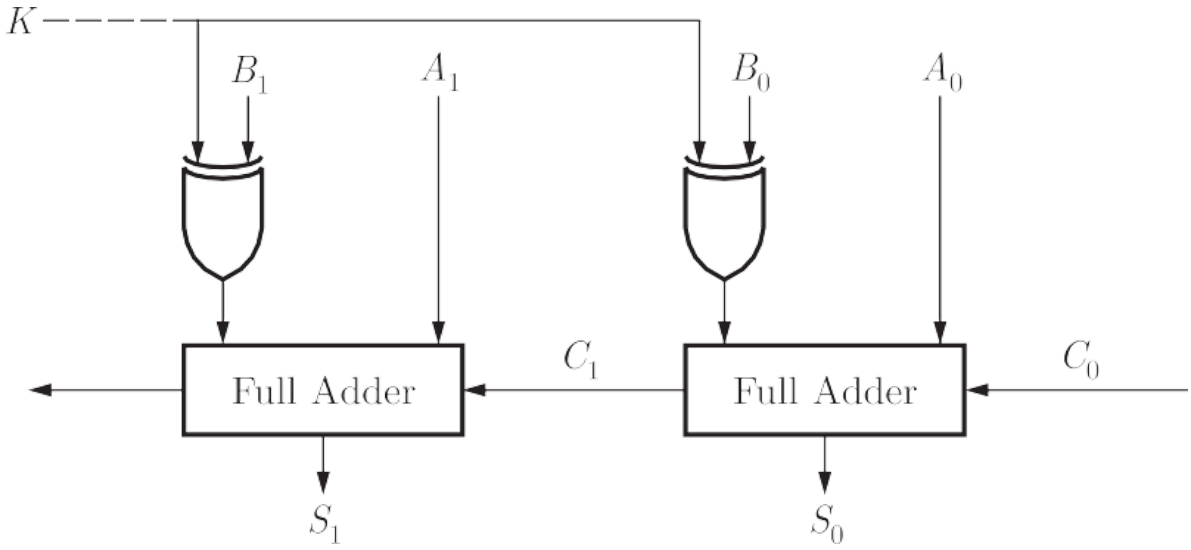
4. Q: For a pipelined CPU with a single ALU, consider the following situations: 1. The j + 1st instruction uses the result of j th instruction as operand. 2. The execution of a conditional jump instruction. 3. The j – th and j + 1 st instructions require the ALU at the same time. Which of the above can cause a hazard?

- 1 and 2 only
- 2 and 3 only
- 3 only
- All the three

5. Q: Consider the ALU shown below: If the operands are in 2's complement representation, which of the following operations can be performed by suitably setting the control lines K and Co only (+ and - denote addition and subtraction respectively)?

- A + B, and A − B, but not A + 1
- A + B, and A + 1, but not A
- A + B, but not A − B, or A + 1
- A + B, and A − B, andA + 1

ALU Image:



6. Q: Which of the following addressing modes are suitable for program relocation at run time? 1. Absolute addressing 2. Based addressing 3. Relative addressing 4. Indirect addressing

- 1 and 4
- 1 and 2
- 2 and 3
- 1, 2 and 4

7. Q: A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

- 120.4 microseconds
- 165.5 microseconds
- 160.5 microseconds
- 590.0 microseconds

8. Q: Match List-I with List-II as shown in the table below and select the correct answer using the codes given below the lists:

- A:3 B:2 C:1
- A:1 B:3 C:2
- A:2 B:3 C:1
- A:1 B:2 C:3

Table (Match List-I with List-II)

List-I	List-II
A. $A[1] = B[j];$	1. Indirect addressing
B. while [* A ++];	2. Indexed addressing
C. int temp=*x ;	3. Auto increment

9. Q: A 5 stage pipelined CPU has the following sequence of stages: IF- Instruction fetch from instruction memory, RD-Instruction decode and register read, EX- Execute: ALU operation for data and address computation, MA-Data memory access-for write access the register read at RD stage it used, WB- register write back. Consider the following sequence of instruction: I1 : LRo, Locl; Ro <= M [Locl], I2: ARo, Ro; Ro <= Ro + Ro I3: AR2, Ro; R2 <= R2 – Ro, Let each stage takes one clock cycle. What is the number of clock cycles to be taken to complete the above sequence of instruction starting from the fetch of I1?

- 8
- 12
- 10
- 15

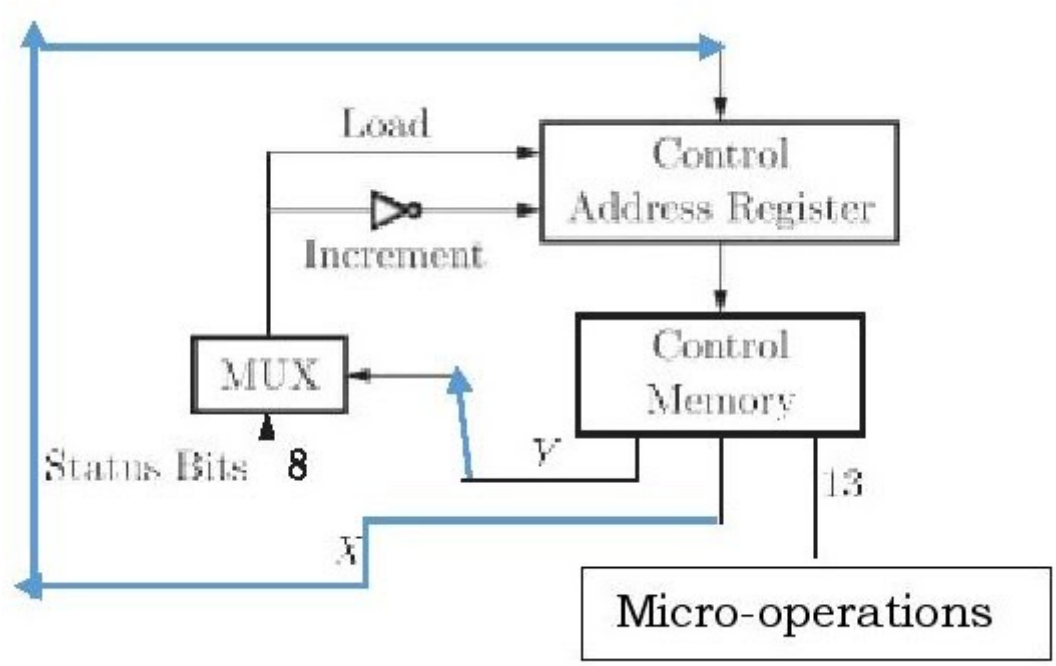
10. Q: Consider a pipelined processor with the following four stagesIF: Instruction FetchID: Instruction Decode and Operand Fetch EX: ExecuteWB: Write Bank as also discussed in thr previous question. The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions? ADD R2, R1, R0 R2 = R1+ R0 MUL R4, R3, R2 R4 = R3*R2 SUB R6, R5, R4 R6 = R5–R4

- ○ 7
- ○ 8
- ○ 10
- ○ 14

11. Q: The microinstructions stored in the control memory of a processor have a width of 26 bits as shown in figure below. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX. How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

- ○ 10, 3, 1024
- ○ 8, 5, 256
- ○ 5, 8, 2048
- ○ 10, 3, 512

Figure (Micro-operations)



12. Q: A CPU has five-stages pipeline and runs at 1GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes pow(10, 9) instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, then total execution time of the program is

- 1.0 second
- 1.2 seconds
- 1.4 seconds
- 11.6 seconds

13. Q: Which of the following are NOT true in a pipe lined processor? (1): Bypassing can handle alll Raw hazards. (2): Register renaming can eliminate all register carried WAR hazards. (3): Control hazard penalties can be eliminated by dynamic branch prediction.

- ◯ 1 and 2 only
- ◯ 1 and 3 only
- ◯ 2 and 3 only
- ◯ 1, 2 and 3

14. To ensure the data-lock condition in a pipeline (without forwarding), the conflict of an instruction in the OF stage is checked with:

- ◯ Only EX stage
- ◯ Only EX and RW stages
- ◯ Only EX and MA stages
- ◯ EX, MA and RW stages
- ◯ None of the above

Thank you for attending your sessional. All the best for your score. Marks will be sent to you after verification of your answers from hand written PDF solutions file, submitted by you through Google Classroom, If no PDF will be uploaded zero marks will be awarded without any reason.

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