NATIONAL INSTITUTE OF TECHNOLOGY KURUKSHETRA

THEORY EXAMINATION
Question Paper

Month and Year of the Examination: **NOV/DEC 2021**

Programme: **B.Tech**/M.Tech/MBA/MCA Semester: - **3rd Semester (CO)**

Subject: - **Computer Organization and Architecture**

Course No: - **CSPC-29** Maximum Marks: **50**

Number of Questions to be attempted: **5** Time allowed: **2 Hours**

Total No. of Questions: **6** Total No. of Pages used: **3**

Unless stated otherwise, the Symbols have their usual meanings in context with subject. Assume suitably and state, additional data required, if any. The Candidates, before starting to write the solutions, should please check the question Paper for any discrepancy, and also ensure that have been delivered the question paper of right **course no**. and right **subject title**.

1. Q(a) Consider computing the overall CPI for a machine A for which the following performance measures are recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz. Assuming the execution of 100 instructions, Calculate the overall CPI. — 5

Instruction Category	Percentage of occurrence	No. of cycles per instruction
ALU	38	1
Load & store	15	3
Branch	42	4
Others	5	5

Q(b) Suppose that the same set of benchmark programs considered above were executed on another machine, call it machine B, for which the following measures were recorded. — 5

Instruction Category	Percentage of occurrence	No. of cycles per instruction
ALU	35	1
Load & store	30	2
Branch	15	3
Others	20	5

What is the MIPS rating for the machine considered in the previous example (machine A) and machine B assuming a clockrate of 200 MHz?

	Or Explain how instruction set, compiler technology, CPU implementation and control and cache and memory hierarchy affect CPU performance and justify the effects in terms of program length, clock rate and effective CPI.	5
2. Q (a)	Consider the execution of a program of 15,00,000 instructions by a linear pipeline processor with a clock rate of 1000 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-0f-sequence executions are ignored. i. Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow through delay. ii. What are the efficiency and throughput of this pipelined processor?	2.5 2.5
Q (b)	A non-pipelined processor X has a clock rate of 250 MHz and an average CPI (cycles per instruction) of 4. Processor Y, an improved successor of X, is designed with 5-stage linear instruction pipeline. However, due to latch delay and clock skew effects, the clock rate of Y is only 200 MHz. i. If a program containing 1000 instructions is executed on both processors, what is the speedup of processor Y compared with that of processor X? ii. Calculate The MIPS rate of each processor during the execution of this particular program.	2.5 2.5
3. Q (a)	Explain the following terms associated with cache design: i. Write-through versus write-back caches. ii. Cacheable versus non-cacheable data. iii. Private caches versus shared caches. iv. Factors affecting cache hit ratios. v. Cache flushing policies.	5
Q(b)	Consider a cache (M_1) and memory (M_2) hierarchy with the following characteristics: M_1: 64K words, 5 ns access time. M_2: 4M words, 40 ns access time. Assume 8-word cache blocks and a set of 256 words with set-associative mapping. i. Show the mapping between M_1 and M_2. ii. Calculate the effective memory-access time with a cache hit ratio of $h = 0.95$.	2.5 2.5

4. Q	The main memory of a computer is organized as 64 blocks, with a block size of 8 words. The cache has 8 block frames. In parts (i) through (iv), show the mapping from the numbered blocks in main memory to the block frames in the cache. Draw all lines showing the mapping as clearly as possible. i. Show the direct mapping and the address bits that identify the tag field, the block number, and the word number. ii. Show the fully associative mapping and the address bits that identify the tag field and the word number. iii. Show the two-way set-associative mapping and the address bits that identify the tag field, the set number, and the word number. iv. Show the sector mapping with four blocks per sector and the address bits that identify the sector number, the block number, and the word number.	10
5. Q	A two-level memory system has eight virtual pages on a disk to be mapped into four page frames (PFs) in the main memory. A certain program generated the following page trace: 1, 0, 2, 2, 1, 7, 6, 7, 0, 1, 2, 0, 3, 0, 4, 5, 1, 5, 2, 4, 5, 6, 7, 6, 7, 2, 4, 2, 7, 3, 3, 2, 3 i. Show the successive virtual pages residing in the four page frames with respect to the above page trace using the LRU replacement policy. Compute the hit ratio in the main memory. Assume the PFs are initially empty. ii. Repeat part (a) for the circular FIFO page replacement policy. Compute the hit ratio in the main memory. iii. Compare the hit ratio in parts (a) and (b) and comment on the effectiveness of using the circular FIFO policy to approximate the LRU policy with respect to this particular page trace.	10
6. Q	Consider a two-level memory hierarchy, M_1 and M_2. Denote the hit ratio of M_1, as h. Let C_1 and C_2 be the costs per kilobyte, S_1 and S_2 the memory capacities, and t_1 and t_2 the access times, respectively. i. Under what conditions will the average cost of the entire memory system approach C_2? ii. What is the effective memory-access time t_a of this hierarchy? iii. Let $r = \frac{t_2}{t_1}$ be the speed ration of the two memories. Let $E = \frac{t_1}{t_a}$ be the access efficiency of the memory system. Express E in terms of r and h. iv. What is the required hit ratio h to make $E > 0.95, if\ r = 100$?	10

@@@@@@@@@@@@@@@@@@@@@@@@@@END@@@@@@@@@@@@@@@@@@@@@@@@@@