MID SEM-II

ITPC 203: Computer Organization and architecture

Max marks:20

Q1 A virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block sizes of 1K words. The following page reference changes occur during time interval. (Only page changes are listed. If the same page is referenced again, it is not listed twice).

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is (i) FIFO (ii) LRU (5 marks)

Q2 The access time of cache memory is 100 ns and that of the main memory is 1000 ns. It is estimated that 80% of the memory requests are for read and others are for write. The hit ratio for reading only accesses is 0.9. A write through procedure is used. (6 marks)

(i) What is the average access time of the system considering only memory read cycles?
(ii) What is the average access time of the system for both read and write requests?
(iii) What is the hit ratio taking in to consideration for Write cycles?

Q3 An instruction at address 021 in the basic computer has I = 0, an operation code of the AND instruction, and an address part equal to 083 (all numbers are in hexadecimal). The memory word at address 083 contains the operand B8F2 and the content of AC is A937. Using instruction cycle, determine the contents of the following registers at the end of the execute phase: PC, AR, DR, AC, and IR. Repeat the problem six more times starting with an operation code of another memory-reference instruction (9 marks)

or

Describe the Instruction cycle state diagram with interrupts (6 marks)