NATIONAL INSTITUTE OF TECHNOLOGY, KURUKSHETRA
THEORY EXAMINATION
Question Paper

Month and year of the Examination: Nov.-Dec.-2024	**Programme: B.Tech.**
Semester: - 4th Semester	**Subject: - Computer Organization and Architecture**
Course No: ITPC 203	**Number of Questions to be Attempted: 5**
Maximum Marks: - 50	**Total No. of Questions: 8**

Q1.

a) Discuss the Von Neumann architecture. How does it differ from the Harvard architecture? **(6 marks)**

b) Explain the role of the bus in connecting different components of the computer system. **(4 marks)**

Q2 What are the different types of addressing modes in an instruction set? Provide examples for each type **(10 marks)**

Q3

a) What are data hazards and control hazards in pipelining? Discuss techniques to handle these hazards. **(6 marks)**

b) Explain how branch prediction works to improve pipelining performance **(4 marks)**

Q4

a) Explain the role of registers in a CPU. What are the different types of registers used in computer architecture? **(6 marks)**

b) Discuss the function of the Program Counter (PC) and the Instruction Register (IR). **(4 marks)**

OR

Q4 A CPU executes instructions with the following cycle times: **(10 marks)**

- Fetch: 4 clock cycles
- Decode: 3 clock cycles
- Execute: 5 clock cycles
- Memory Access (if needed): 2 clock cycles

If the processor is executing a sequence of 10 instructions, where every instruction involves fetching, decoding, and executing, but only the 5th and 8th instructions require a memory access, how many total clock cycles are required to complete all 10 instructions?

Q5 Given the reference string of pages: **(10 marks)**

1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5

How many page faults occur using the FIFO, LRU, and Optimal page replacement algorithms if there are 3-page frames?

OR

Q5 For a system with 4-page frames and the following reference string of pages: **(10 marks)**

1, 2, 3, 1, 4, 2, 1, 5, 6, 2, 3, 4

- How many page faults occur using the FIFO algorithm?
- Calculate the hit ratio

Q 6 Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs: **(10 marks)**

Instruction Type	Instruction Count	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine B		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

a) Determine the effective CPI, MIPS rate, and execution time for each machine.
b) Comment on the results.

OR

Q6 Consider a 5-stage pipeline with hazards. The instructions are as follows: **(10 marks)**

1. I1: ADD R1, R2, R3
2. I2: SUB R4, R1, R5
3. I3: MUL R6, R2, R7

If there are data hazards between the instructions, how many cycles would it take to complete all three instructions if the pipeline includes forwarding and stalls when necessary?

Q7

a) In a paging system with a page size of 1 KB and a logical address space of 64 KB, how many pages will be needed to address the entire logical address space? **(6 marks)**

b) In a system with a memory size of 16 MB, how many pages and page table entries are required if the page size is 4 KB? **(4 marks)**

Q8

a) Explain the concept of Direct Memory Access (DMA). How does it improve the performance of a system compared to using the CPU for data transfer? **(6 marks)**

b) Explain the process of DMA request and acknowledge in a system that uses DMA. **(4 marks)**