Roll No _____

Department of Computer Engineering
CSPC-20 (Operating Systems)
Mid-Sem II Examination (Date: 19/04/2023)

Time: 50 min

Marks: 15

1. Consider two processes P1 and P2 accessing the shared variables X and Y protected by two binary semaphores SX and SY respectively, both initialized to 1. P and V denote the usual semaphore operators, where P decrements the semaphore value, and V increments the semaphore value. The pseudo-code of P1 and P2 is as follows:

P1:	P2:

while true do {
L1 : .....
L2 : .....
X = X + 1;
Y = Y - 1;
V(SX);
V(SY);
}
	while true do {
	L3 : .....
	L4 : .....
	Y = Y + 1;
	X = Y - 1;
	V(SY);
	V(SX);
	}

In order to avoid deadlock, what is the correct operators at L1, L2, L3 and L4 respectively.

OR

1'. Write and explain the Banker's algorithm for finding out the safe state in order to allocate resources while avoiding deadlock in a system with multiple instances of the resources. **(3)**

2. Give a solution to Readers-Writers problem using Monitors. **(2)**

3. The following page addresses, in the given sequence, were generated by a program:
1 2 3 4 1 3 5 2 1 5 4 3 2 3
This program is run on a demand paged virtual memory system, with main memory size equal to 4 pages. Indicate the page references for which page faults occurs for the LRU page replacement algorithm. Assume that the main memory is empty initially. **(3)**

4. Given six memory partitions of 100 MB, 170 MB, 40 MB, 205 MB, 300 MB, and 185 MB (in order), how would the first-fit algorithm places processes of sizes 200 MB, 15 MB, 185 MB, 75 MB, 175 MB, and 80 MB (in order)? Indicate which—if any—requests cannot be satisfied. **(2)**

5. Consider a demand-paging system with a paging disk that has an average access and transfer time of 20 milliseconds. Addresses are translated through a page table in main memory, with an access time of 1 microsecond per memory access. Thus, each memory reference through the page table takes two accesses. To improve this time, a TLB is added that reduces access time to one memory reference if the page-table entry is in the TLB. Assume that 80 percent of the accesses are in the associative memory and that, of those remaining, 10 percent (or 2 percent of the total) cause page faults. What is the effective memory access time?

OR

5'. Consider a demand paging system. It takes 4 milliseconds to service a page fault if an empty frame is available or if the replaced page is not modified and 10 milliseconds if the replaced page is modified. Memory-access time is 100 nanoseconds. Assume that the page to be replaced is modified 80 percent of the time. What is the maximum acceptable page-fault rate for an EAT of no more than 200 nanoseconds? **(3)**

6. Consider a system with 2-byte-addressable main memory, 32 bit logical addresses, 4 kilobyte page size and page table entries of 4 bytes each. What is the size of the page table in the system in megabytes? **(2)**