National Institute of Technology, Kurukshetra
B.Tech (Information Technology/AI/M&C) IV Semester
Mid Sem Exam-II April 2025, Operating Systems

Time: 50 min MM: 15

Instructions: Attempt all questions.

1. a) Consider a single level paging scheme. The virtual address space is 256 MB and page table entry size is 4 bytes. What is the minimum page size possible such that the entire page table fits well in one page? (3)

   b) Consider a system using multilevel paging scheme. The page size is 1 MB. The memory is byte addressable and virtual address is 64 bits long. The page table entry size is 4 bytes. Find-(I)How many levels of page table will be required? (ii)Give the divided physical address and virtual address. (4)

2. a) What is Thrashing. Describe the methods to avoid it (2)

   b) A system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (LRU) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string -4 , 7, 6, 1, 7, 6, 1, 2, 7, 2
   Also calculate the hit ratio and miss ratio. (2)

3. a) What is the purpose of valid invalid bit in virtual memory management. (2)

   b) With a neat diagram, explain the process of virtual to physical address translation using an inverted page table. (2)