NATIONAL INSTITUTE OF TECHNOLOGY KURUKSHETRA
THEORY EXAMINATION
Question Paper

Month and Year: Nov/Dec 2024	**Programme: B.Tech. (ECE)**
Semester 3rd	**Subject: Electronic Devices and Circuits**
Course No.: ECPC-201	**Maximum marks: 50**
Number of questions to be attempted: 05	**Time allowed: 3 Hrs.**
Total no. of questions: 05	**No. of pages used: 02**

NOTE: Attempt all questions. Assume suitable data if required.

Q.1 (a) Discuss and differentiate between Avalanche and Zener breakdown mechanism. Also draw diode equivalent circuit models. [5]

(b) Determine the currents I_1, I_2, and I_{D2} for the network of Fig. 1. [5]

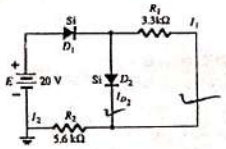

Fig. 1

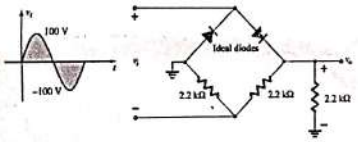

Fig. 2

Q. 2 (a) Sketch V_0 for the network of Fig. 2 and determine the dc voltage available. [5]

(b) Determine V_0 for each network of Fig. 3 for the input shown. [5]

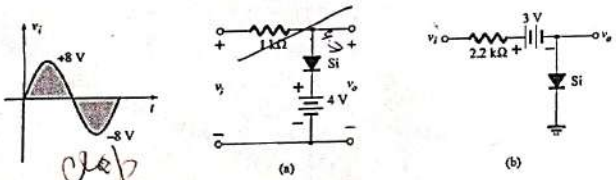

Fig. 3

Q. 3 (a) For the collector-feedback configuration of Fig. 4, determine: I_B, I_C and V_C. [5]

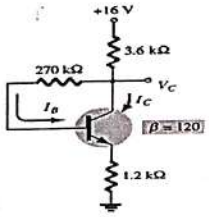

Fig. 4

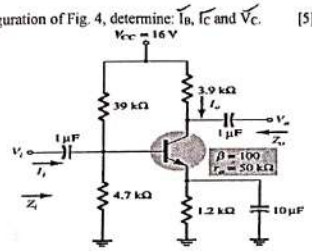

Fig. 5

(b) For the network of Fig. 5: [5]
(i) Determine r_e (ii) Find Z_i and Z_o (with $r_o = \infty\Omega$)
(iii) Determine A_v (with $r_o = \infty\Omega$) (iv) Repeat parts *(iii)* including $r_o = 25$ kΩ.

Q. 4 (a) Derive the expression of input impedance, output impedance, voltage gain and current gain of Common-Emitter configuration using complete hybrid model. [5]

(b) Explain the working of n-channel MOSFET stating depletion, weak and strong inversion conditions. Also draw the I-V characteristics. [5]

Q.5 (a) Derive the expression of input impedance output impedance, voltage gain of common-source MOSFET configuration. [5]

OR

(b) Explain the working of phase shift oscillator and derive the expression of frequency.

(c) Briefly explain the working of n-channel JFET. Also describe the following terms in connection to the MOSFET: [5]

i. Channel length modulation
ii. Drain Induced Barrier Lowering

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