DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
B.TECH. ECE, 4th SEMESTER, MID-SEMESTER EXAM-FEB.2026
SUBJECT: Computer Architecture COURSE CODE: ECPC-211

Maximum Marks: 15 Time: 50 minutes Roll Number.....

1. A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one-address instructions can be formulated? [2]
2. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is one memory word. [3]
3. Write a program to evaluate the arithmetic statement: [4]

$$X = \frac{A - B + C*(D*E - F)}{G + H*K}$$

a. Using a general register computer with 3 address instructions
b. Using a general register computer with 1 address instructions

S	$C_{in} = 0$	$C_{in} = 1$
0	$D = A + B$ (add)	$D = A + 1$ (increment)
1	$D = A - 1$ (decrement)	$D = A + \bar{B} + 1$ (subtract)

Fig.1

4. Consider a 16-bit processor, an instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) relative; (c) register indirect; (d) index with R1 as the index register. [2]
5. An ISA with 8-bit Floating Point Representation(1 sign bit, four bits exponent, three bits fraction/Significand). Find range for normalized and denormalized values, also the representations of 0, NaN, infinity. Prove that floating point numbers are not distributed evenly on the number line. [4]

OR

Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations(**see Fig.1**) in conjunction with the input carry C_{in}. Draw and explain the complete circuit for the first two stages.