Reg. No.:

Name :

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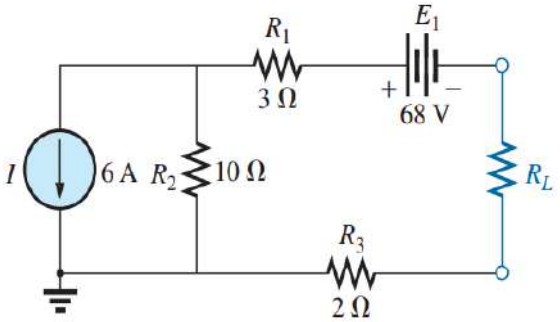
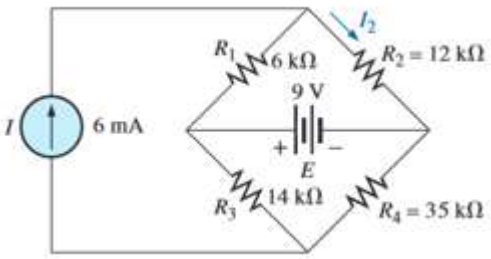
Mid-Term Examinations – October 2021

Programme	:	**B. Tech.**	Semester	:	**Fall 2021-22**
Course	:	**Electric Circuits & Systems**	Code	:	**EEE1001**
Faculty	:	**Mr. Amit Kumar Singh**	Slot/ Class No.	:	**A11+A12+A13/0600**
Time	:	**1 ½ hours**	Max. Marks	:	**50**

Answer all the Questions

Q.No.	Sub. Sec.	Question Description	Marks
1	(a)	Derive the condition for the maximum power transfer in a given circuit.	**4**
	(b)	Determine the value of R_L for the maximum power transfer as shown in Figure 1, also find the maximum power transferred to the load.  Figure 1	**6**
2	(a)	A series *RLC* circuit with L =160 mH, C = 100 µF, and R = 40.0Ω is connected to a sinusoidal voltage V (t) = 40sinωt, with ω = 200 rad/s. 1. What is the impedance of the circuit? 2. Let the current at any instant in the circuit be I (t) = I0 sin (ωt -φ). Find I0. 3. What is the power factor?	**4**
	(b)	Using superposition theorem, determine the current I_2 through R_2 =12 KΩ resistor for the circuit shown in Figure 2.  Figure 2	**6**

3 (a) Determine the value of "V_0 & I" in the circuit shown in Figure 3 considering the diodes approximate ideal. **4**

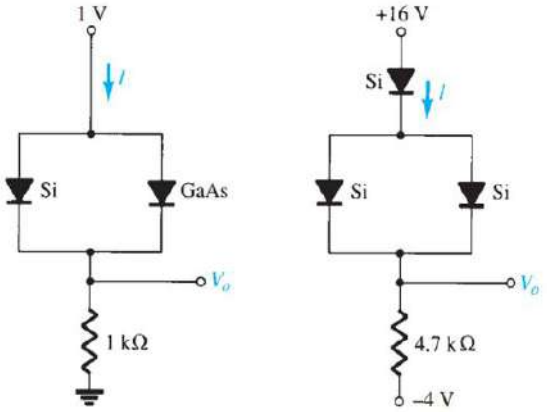


Figure 3

(b) Determine the output waveform (V_0) in the network shown in Figure 4 and calculate the output D.C level and required PIV of each diode? **6**

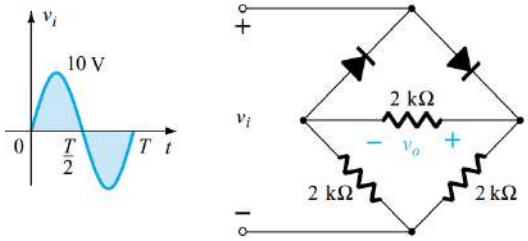


Figure 4

4 (a) Draw the input/ output characteristics of the CE configuration NPN transistor made up with silicon. Also define the term I_{CEO} **5**

(b) Explain the working of n-channel D-MOSFET with the transfer characteristics curve **5**

5 (a) Design a combinational logic circuit with 3 input variables that will produce logic '1' output when more than one input variables are at logic '0'. **5**

(b) Minimize the following Boolean function using K-map and realize it using NAND gates only **5**

$$F(A, B, C, D) = \sum (0,2,5,7,11,14)$$

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