

Roll No. 22001003029

Total Pages : 3

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December 2023
B.Tech. IIIrd SEMESTER
Digital Electronics (ESC-302)

Time : 3 Hours]

[Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART-A

1. (a) Draw only logic diagram of full adder. (1.5)
(b) Convert $(265.731)_8 = ()_{10}$. (1.5)
(c) Give the definition of Multiplexer. (1.5)
(d) What is Modulus Counter? (1.5)
(e) What are the advantages of CMOS logic families used for implementing logic gates? (1.5)
(f) What is Race-around condition in flip-flop? (1.5)
(g) Enlist significant specifications of ADCs. (1.5)

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- (h) Find the output voltage of a 4-bit ladder, having digital input 0110. Assume logic 0 = 0V and logic 1 = 10V. (1.5)
- (i) What is the purpose of using PLD? (1.5)
- (j) What is sequential memory ? (1.5)

PART-B

2. (a) Minimize the following function using K-map. (10)

$$F(A,B,C,D) = \sum m(0,1,2,3,4,5,6,11)$$
- (b) Design two-bit comparator and draw logic diagram. (5)
3. (a) Explain clocked RS flip-flop with operation. (5)
- (b) Explain 3-bit asynchronous counter with diagram and draw timing diagram. (10)
4. (a) What are the error detection and correction codes? (15)
- (b) Simplify the following three-variable expression using Boolean algebra: $Y(A,B,C) = \sum m(0,2,4,6)$
- (c) Convert $(A23.4E)_{16} = ()_2$
- (d) Interfacing CMOS and TTL Devices.
- (e) Convert $(100011110)_2 = ()_{10}$
5. (a) Differentiate between CPLD and FPGA. (5)

- (b) Briefly explain the working of Dynamic RAM cell. Also explain MROM, PROM, EPROM, EEPROM. (10)

6. (a) Implement the following function using 8:1 MUX

$$F(A,B,C,D) = \sum m(0,2,3,6,8,9,12,14)$$
 (10)
- (b) Explain universal Register with suitable diagram. (5)
7. Explain 3-bit weighted resistor type DAC, comparator with suitable diagram. And give its advantages and disadvantages and give specifications of DAC. (15)