JC Bose University of Science and Technology, YMCA, Faridabad

First session Exam, Subject: Digital Electronics

B. Tech CE31 3rd Sem (Computer Engineering)

**Duration: 90 min** **M. Marks: 30**

**Note: All Question Carry Equal Marks**

1. You are given the data bits 1011 and asked to encode them using the Hamming (7,4) code, which uses 4 data bits and 3 parity bits. Also, assume that a single-bit error occurs during transmission. Find the transmitted code, detect the error, and correct it? (CO-1, HO)
2. Design a 256-to-1 multiplexer using 16-to-1 multiplexers. Explain the process step by step, including the number of multiplexers used, how the inputs are organized, how the selection lines are assigned, and the final output selection. Include a diagram to illustrate your design? (CO-2, IO)
3. Explain ripple counter in detail? (CO-2, IO)
4. Explain the working of SR flip flop in detail? (CO-2, LO)

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J. C. BOSE UNIVERSITY OF SCIENCE AND TECHNOLOGY, YMCA, FARIDABAD

SESSIONAL-I (October 2024) (CE-III Sem)

Digital Electronics (ESC-302)

MM:15 Time: 90 min

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|---|---|---|---|---|
| Q1 | a) A transmitter uses a single error-correcting code for the message using even parity. The message received at the receiving end is 1110101. Check and correct the error. | (2) | CO1 | HOCQ |
| | b) Perform the operation 8-9 by using 2's complement method: | (2) | CO1 | IOCQ |
| Q2 | a) Minimize the following expressions using k-map: $Y(A,B,C,D) = \sum m(0,2,4,7,8,10,12,13) + d(3,15)$ and implement it using logic gates. | (2) | CO1 | IOCQ |
| | b) Draw and explain BCD Adder. | (3) | CO2 | LOCQ |
| | c) Implement the following expression using a single 8:1multiplexer $Y(A,B,C,D) = \sum m(0,2,3,6,8,9,12,14)$ | (3) | CO2 | HOCQ |
| Q3 | Design a 3-bit Binary-to-Gray code converter using a PLA. | (3) | CO4 | IOCQ |

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**JC Bose University of Science and Technology, YMCA, Faridabad**
**Second session Exam, Subject: Digital Electronics**
**B. Tech CE31 3rd Sem (Computer Engineering)**

**Duration: 90 min** **M. Marks: 30**

**Note: All Question Carry Equal Marks**

1. Explain Dual Slope A/D converter in detail? (CO-3, HO)
2. Design a 3-bit synchronous counter using JK flip flop (CO-2, IO)
3. Compare Weighted Resistor DAC, R-2R Ladder DAC, and Current Steering DAC based on their working principles, accuracy, and applications? (CO-2, IO)
4. Design a 2048X8 memory using 256X8 memory chips? (CO-4, IO)