- 6. Explain Address sequencing in micro programmed control unit with a suitable block diagram. (15)
- 7. Explain in detail Control Dependency (Branch Hazards) and Data Hazards. (15)

Roll No. ....

Total Pages: 4

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## December 2023 B.Tech. (CE DS) V SEMESTER Computer architecture (PCC-DS-503)

Time: 3 Hours]

[Max. Marks: 75

## Instructions:

- 1. It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.
- 2. Answer any four questions from Part-B in detail.
- 3. Different sub-parts of a question are to be attempted adjacent to each other.

## PART-A

- 1. (a) What are the benefits of studying computer architecture? (1.5)
  - (b) Explain locality of reference principle in cache memory. Why secondary memory is used in computer system? (1.5)
  - (c) What is the role of control memory in micro programmed control unit? (1.5)
  - (d) Why registers are used in computers? (1.5)
  - (e) Compare register stack and memory stack. (1.5)
  - (f) What is bus arbitration? (1.5)

- (g) Explain direct addressing mode and indirect addressing mode. (1.5)
- (h) Let SP = 0000 in the stack. How many items are there in the stack of FULL = 1 and EMPTY = 0? (1.5)
- (i) Explain a bus system for four registers that uses multiplexers. (1.5)
- (j) Why Input-Output interface is required for peripheral devices? Explain. (1.5)

## PART-B

- 2. (a) When do you say the floating point number is normalized? Consider two normalized floating-point numbers 0.9504\*10 and 0.8200\*10 Find their sum and normalized the result. (10)
  - (b) (a) Specify the micro operation for the given below: (5)
    - (i) AC ← DR
- idona not (ii) PC PC + 1 addended and one stadW (a)
  - (b) Draw the control word format for the given instruction:
  - (i) R1 ← R2 + R3
  - (ii) R4 ← R4 ∨ R5
- 3. Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating the numerical result:

  (5)

(b) A virtual memory system has an address space of 16k words, a memory space of 8k words, and page and block size of 2k words. The page address trace of a program has been found to be 7 5 3 2 1 0 4 1 6 7 4 2 0 1 3 5. Determine the 4 pages that are resident in main memory after each page reference change if the replacement algorithm used is (10)

- (i) FIFO
- (ii) LRU.

4. Write short notes on the following: (15)

- (i) Handshaking.
- (ii) Interrupts.
- (iii) Paged segment memory.
- (a) Describe DMA with suitable block diagram. Why
  does DMA have priority over the CPU when both
  request a memory transfer? Explain.
  - (b) What is hit ratio? How is it used to improve the performance of cache memory. A two-way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K × 32.
  - (i) Formulate all important information required to construct the cache memory.
  - (ii) What is the size of cache memory? (10)

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