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305504

December, 2019

B.Tech. (ECE) - V SEMESTER

CMOS Design (ECEL501)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART - A

1. (a) Differentiate between MOS as resistance and MOS as current source configuration. (1.5)

(b) What is threshold voltage of MOS device? (1.5)

(c) Why selection of W/L ratio of a MOS device is critical? (1.5)

(d) What is the impact of channel length modulation on drain current? (1.5)

(e) What is difference between layout and stick diagrams? (1.5)

(f) What is velocity saturation effect? (1.5)

(g) Design two input or gate using pseudo inverter configuration. (1.5)

(h) What is the meaning of scaling of MOS devices? (1.5)

(i) How subthreshold conduction of MOSFET can be advantageous? (1.5)

(j) How junction leakage of a MOS device can be reduced? (1.5)

PART - B

2. (a) Describe twin tub process for fabrication of the CMOS transistor with suitable diagram. (10)

(b) Explain VLSI design flow with suitable flow chart. (5)

3. (a) Explain various regions of operation for NMOS. Derive the expression for the drain current in various region of operation for NMOS. (8)

(b) Explain RC delay model and linear delay model of CMOS circuits. (7)

4. (a) What is transmission gate logic? Why it is preferred over NMOS/PMOS switch? Design 4 × 1 Mux using transmission gate logic. (8)

(b) Using an example enlist the various steps for designing a sequential CMOS logic circuit. (7)

5. (a) What is the rise time and fall time of CMOS inverter? Explain using necessary expression. (8)

(b) Explain the static and dynamic power dissipation in CMOS circuits with necessary diagram and expression. (7)

6. (a) Explain the operation of CMOS dynamic logic. What is the cascading issue in dynamic logic circuits? (8)

(b) What is NMOS inverter? Explain the different form of pull up. (7)

7. (a) What is latch up? How it can be reduced? (5)

(b) Draw circuit and stick diagram for half subtractor using CMOS combinational logic design. (10)