Roll No. ..... Total Pages : 3

017301

December 2023

B.Tech. EEIoT – III SEMESTER

Digital Electronics (EEN–301)

Time : 3 Hours] [Maximum Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any **four** questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*
4. *Assume relevant data, if required.*

PART–A

1. (a) Implement Ex-or gate using CMOS Logic. (1.5)

   (b) Perform the following:

   (i) A2.34 – 91.12 (ii) A2.34 = $(\ )_{BCD8421}$ (1.5)

   (c) How decoder is different from Demultiplexer? (1.5)

   (d) What is the difference between Discrete signals and Digital signals? (1.5)

   (e) Mention application of Shift Registers. (1.5)

(f) Make a MOD-24 counter essentially using MOD-12 counter. How many JK flip flop now it has in place? (1.5)

(g) Write the excitation table of SR flip flop. (1.5)

(h) Draw the diagram of NOT gate using NMOS. (1.5)

(i) What is the merit of using schottky diodes in logic families? (1.5)

(j) How many comparators are required to build a 5-bit simultaneous A/D converter? (1.5)

PART–B

2. (a) Minimize the following using Quine Mcluskey method :

$f(A,B,C,D) = \pi M(1,2,3,8,9,8,10,11,14) + d(7,15)$. (7)

(b) The seven bit data to be transmitted is 011 0101. Assume that even parity has been used using Hamming Code. Check is it correct or not. If not find the correct code. (8)

3. (a) Design a 64:1 multiplexer using only and only 16:1 multiplexer. (10)

(b) Design a 3 bit full subtractor using 4 bit adder. (5)

4. (a) Design MOD-11 up counter. (7)

(b) Explain the working of 8-bit Shift Register (Serial in-Parallel out). (8)

5. (a) Explain the NOR gate Logic using of TTL Family, illustrating its merit over other family. (5)

(b) Draw NOR gate using CMOS Logic. (5)

(c) Explain the sourcing and sinking current circuit used in logic families. (5)

6. (a) Explain the Analog to Digital conversion time of a Dual Slope ADC, A 12 bit Dual-Slope ADC has clock frequency 10 MHz. What could be the maximum conversion time? (10)

(b) Explain the working of Successive Approximation ADC. (5)

7. (a) What is operational difference between an SRAM and DRAM? (8)

(b) Describe the difference between PAL and FPGA. (7)
